CLAIMS

1. A method for calculating metrics of a trellis function in a digital signal processor, comprising the steps of:

in response to a trellis instruction that specifies locations of trellis state metrics for a time t_0 and transition metrics from time t_0 to time t_1, for selected trellis states, adding a transition metric to a first state metric for time t_0 to provide a first value and subtracting the transition metric from a second state metric for time t_0 to provide a second value;

for each selected trellis state, comparing the corresponding first and second values; and

selecting the maximum of the corresponding first and second values for each selected trellis state to provide trellis state metrics for time t_1.

2. A method as defined in claim 1, further comprising the step of, for each selected trellis state, adding to the maximum value a correction factor that is a function of the corresponding first and second values.

3. A method as defined in claim 2, wherein the step of adding a correction factor comprises accessing a lookup table containing correction factors.

4. A method as defined in claim 1, wherein the trellis instruction implements a forward trellis function for calculating α trellis state metrics.

5. A method as defined in claim 1, wherein the trellis instruction implements a reverse trellis function for calculating β trellis state metrics.

6. A method as defined in claim 1, wherein the trellis instruction simultaneously implements a forward trellis function for calculating α trellis state metrics and a reverse trellis function for calculating β trellis state metrics, using a single instruction, multiple data approach.

7. A method for calculating metrics of a trellis function in a digital signal processor, comprising the steps of:

in response to α metrics for a time t_0 and transition metrics from time t_0 to time t_1 specified by a trellis instruction, calculating an α metric for selected trellis states for time t_1, and

in response to β metrics for a time t_2 and transition metrics from time t_2 to time t_1 specified by the trellis instruction, calculating a β metric for the selected trellis states for time t_1.

8. A method as defined in claim 7, wherein the step of calculating an α metric for the selected trellis states comprises the steps of:

for each selected trellis state, adding a transition metric to a first α metric for time t_0 to provide a first value and subtracting the transition metric from a second α metric for time t_0 to provide a second value;

for each selected trellis state, comparing the corresponding first and second values; and

selecting the maximum of the corresponding first and second values for each selected trellis state to provide α metrics for time t_1.

9. A method as defined in claim 8, wherein the step of calculating an α metric for the selected trellis states further comprises the step of, for each selected trellis state, adding to the maximum value a correction factor that is a function of the corresponding first and second values.

10. A method as defined in claim 7, wherein the step of calculating a β metric for the selected trellis states comprises the steps of:

for each selected trellis state, adding a transition metric to a first β metric for time t_2 to provide a first value and subtracting the transition metric from a second β metric for time t_2 to provide a second value;

for each selected trellis state, comparing the corresponding first and second values; and

selecting the maximum of the corresponding first and second values for each selected trellis state to provide β metrics for time t_1.

11. A method as defined in claim 10, wherein the step of calculating a β metric for the selected trellis states further comprises the step of, for each selected trellis state, adding to the maximum value a correction factor that is a function of the corresponding first and second values.

12. A method as defined in claim 7, wherein the step of calculating an α metric for the selected trellis states comprises calculating α metrics for a plurality of trellis states in response to a single trellis instruction.

13. A method as defined in claim 7, wherein the step of calculating a β metric for the selected trellis states comprises calculating β metrics for a plurality of trellis states in response to a single trellis instruction.

14. A method as defined in claim 7, wherein the steps of calculating an α metric and calculating a β metric are performed simultaneously.

15. A method for calculating a log MAP function in a digital signal processor, comprising the steps of:

in response to a log MAP instruction that specifies locations of first, second, third and fourth parameters, calculating the sum or difference of the first and second parameters to provide a first value and calculating the sum or difference of the third and fourth parameters to provide a second value;

selecting the maximum of the first and second values; and

adding to the maximum value a correction factor that is a function of the first and second values to provide a log MAP result.

16. A method as defined in claim 15, wherein the step of adding a correction factor comprises accessing a lookup table containing correction factors.

17. A method as defined in claim 15, wherein two or more log MAP results are calculated in response to a single log MAP instruction.

18. A processor comprising:

a memory for storing instructions and operands for digital signal computations;

a program sequencer for generating instruction addresses for fetching selected ones of said instructions from said memory; and

a computation block comprising a register file for temporary storage of operands and results and an accelerator for executing a trellis instruction that specifies locations of trellis state metrics for a time t_0 and transition metrics from time t_0 to time t_1, said accelerator comprising an adder for adding a transition metric to a first state metric for time t_0 to provide a first value and an adder for subtracting the transition metric from a second state metric for time t_0 to provide a second value, a comparator for determining the maximum of the corresponding first and second values for each trellis state and a data selector for selecting the maximum of the corresponding first and second values for selected trellis states.

19. A processor comprising:

a memory for storing instructions and operands for digital signal computations;

a program sequencer for generating instruction addresses for fetching selected ones of said instructions from said memory;

a first computation block comprising a register file for temporary storage of operands and results and an accelerator for executing a trellis instruction in response to α metrics for a time t_0 and transition metrics from time t_0 to time t_1 specified by the trellis instruction, said accelerator comprising means for calculating an α metric for selected trellis states at a time t_1 based on the α metrics for time t_0 and the transition metrics; and

a second computation block comprising a register file for temporary storage of operands and results and an accelerator for executing the trellis instruction in response to β metrics for a time t_2 and transition metrics from time t_2 to time t_1 specified by the instruction, said accelerator comprising means for calculating a β metric for the selected trellis states at time t_1 based on the β metrics for time t_2 and the transition metrics from time t_2 to time t_1.

20. A processor comprising:

a memory for storing instructions and operands for digital signal computations;

a program sequencer for generating instruction addresses for fetching selected ones of said instructions from said memory; and

a computation block comprising a register file for temporary storage of operands and results and an accelerator for executing a log MAP instruction that specifies locations of first, second, third and fourth parameters, said accelerator comprising a first adder for calculating

the sum or difference of the first and second parameters to provide a first value and a second adder for calculating the sum or difference of the third and fourth parameters to provide a second value, a data selector for selecting the maximum of the first and second values, a lookup table for generating a correction factor that is a function of the first and second values, and a third adder for adding the correction factor to the maximum value to provide a log MAP result.

21. An accelerator for use in a digital signal processor computation block, comprising:

a first carry save adder for receiving inputs to the accelerator;

a first full adder for combining sum and carry outputs of the first carry save adder;

a lookup table for generating a correction factor in response to the output of the first full adder;

a multiplexer for selecting one or more of the inputs to the accelerator in response to the sign of the output of the first full adder;

a second carry save adder for adding one or more outputs of the multiplexer and the output of the lookup table; and

a second full adder for combining sum and carry outputs of the second carry save adder.

22. An accelerator as defined in claim 21, wherein the first carry save adder has four inputs, the multiplexer selects two of the four inputs and the second carry save adder has three inputs.

23. An accelerator as defined in claim 22, further comprising a data selector for supplying the sum and carry outputs of the second carry sum adder to the inputs of the first carry sum adder.

24. An accelerator as defined in claim 21, wherein said first carry save adder and said first full adder comprise a first pipeline stage, said lookup table, said multiplexer and said second carry save adder comprise a second pipeline stage and said second full adder comprises a third pipeline stage.